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REGISTRIRANA KOPIJA

	Priimek in ime	Podpis			Gradivo	Odstopi netol. mer	Toplotna obdelava	Površ. zaščita	Pripadnost
Konstr.	Urbančnik	[signature]	Izdaja	1					TRIGLAV
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Pregled.	Rogač	[signature]	Št. obv.	11-002					
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Iskra Delta
proizvodnja računalniških sistemov in inženiring, p.o.

Naziv	List	Stran	J	K	Identifikacijska številka
TESTING PROCEDURE	1				3325 2044

Namembnost kopije	Arhiv	Merilo	Sekcija	Namesto identifikacijske številke
				1884 2044

Prenos tretjim osebam in uporaba v nedogovorjene namene nista dovoljena.

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VME MODULE
CPU 68Ø1Ø

TESTING PROCEDURE

ident: 33.252.Ø44

Preliminary Version: June 1986

TESTING PROCEDURE

Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-002					2				33252044

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proizvodnja računalniških sistemov in inženiring, p.o.

Arhiv

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CHAPTER 1

1. INTRODUCTION

The CPU 68Ø1Ø board(s) can be tested in the stand alone or in the system environment. In the stand alone environment only internal functions of the board(s) can be tested. In the system enviroument internal and external functions of the CPU 68Ø1Ø board(s) can be tested.

The VME CPU 68Ø1Ø TESTING PROCEDURE is written with strong connection to the following literature:

- VME MODULE CPU 68Ø1Ø PACKAGE OF TESTING PROGRAMS (ident: 29.638.Ø44),
- VME MODULE CPU 68Ø1Ø HARDWARE USER'S MANUAL (ident: 29.572.Ø44),
- VME MODULE CPU 6801Ø TECHNICAL MANUAL (ident: 32.8Ø4.Ø44).

See the mentioned literature for additional information about timings, circuit schematics, functioning of PALs and ICs and other dependent information, which will help in testing and troubleshooting of the CPU 68Ø1Ø board(s).

Because of the high speed of the CPU 68Ø1Ø board(s), a good logic analyzer is necessary for fast troubleshooting and error detection, correction of the board(s). Also, good understanding of VME bus principles and MC68ØØØ philosophy is strongly recommended.

CHAPTER 2

2. PREPARATION OF THE CPU 68Ø1Ø BOARD(S) FOR TESTING

The board, which is going to be tested, should be optically carefully examined first, to find out that all elements are positioned correctly, in the right direction, etc.

In the second step statical test of short conections between power supply lines and ground should be tested (+5V, +12, -12 and GND) between each other.

Then, the EPROMs with the resident firmware should be inserted and the CPU 68Ø1Ø board connected to power and grounding, when tested in the stand alone environment, or put into a system, when the CPU 68Ø1Ø board is going to be tested in the system environment.

Some care should be taken, when inserting EPROMs, that they are inserted in proper direction and positions. Right EPROM resident firmware should be choosen, depending on the environment, in which the CPU 68Ø1Ø board is being tested.

A terminal should be connected to the terminal interface connector, with the proper set-up.

When testing in the system environment, the system should be previously fully tested with a good CPU 68Ø1Ø to assure that only the CPU 68Ø1Ø to be tested, is a new component in the system. Also, all programmable logic (PALs, EPROMs) of the CPU 68Ø1Ø being tested, should be fully tested previously.

CHAPTER 3

2. TESTING IN THE STAND ALONE ENVIRONMENT

The internal functions of the CPU 68Ø1Ø board(s) can be tested in the stand-alone environment.

The EPROM resident firmware should be inserted into the CPU 68Ø1Ø board being tested:

- IC EPROM 32K*8 MONU 68Ø1Ø (ident: 32.937.Ø44)
  in the socket on the E16 position,

- IC EPROM 32K*8 MONL 68Ø1Ø (ident: 32.936.Ø44)
  in the socket on the E25 position.

In the stand alone environment the basic internal functions of the CPU 68Ø1Ø board(s) can be tested. The EPROM resident firmware includes System Monitor, Diagnostic Monitor and Test Program of the CPU 68Ø1Ø board. With this EPROM resident firmware the Dynamic RAM, Bus Time Out logic, Memory Management Unit, Parity logic, Interrupts from the CIO, SCC and RTC, the Floating Point Unit, Centronics type of Printer interface connection and other functional units of the CPU 68Ø1Ø board(s) can be tested. Also additional tests can be down-loaded, executed, repeated etc. See the VME MODULE CPU 68Ø1Ø PACKAGE OF TESTING PROGRAMS (ident. 29.638.Ø44) for additional information about executing the tests, repeating them, different print-outs in the case of errors, etc.

After power-up, printing on the terminal should be started. If there is no print-out on the terminal the initial power-up RESET-logic, generation of clocks, select of the EPROM and SCC, gneration of the DTACK- signal, etc., should be checked, until there is a terminal active and the tests can be executed by the terminal interactively.

Initial printing on the terminal requires only proper work of minimal part of the CPU 68Ø1Ø board(s), that is processor MC68Ø1Ø, Memory Management Unit MC68451, ROM/EPROM, SCC, clocks CLKX, CLK and PCLK, and minimum of additional logic. The rest of testing activity can be built up after the minimal part of the CPU 68Ø1Ø board works properly.

If certain test find errors, see the previonsly mentioned literature in CHAPTER 1 for additional information about testing programs, functioning of tested ICs, connections beetween them, etc.

When all tests are executed without errors, testing of the CPU 68Ø1Ø board(s) in the system invironment can be started.

CHAPTER 4

4. TESTING IN THE SYSTEM ENVIRONMENT

After the testing of the tested CPU 68Ø1Ø board(s) in the stand alone environment, the testing in the system invironment can be started.

For the testing in the system environment VME bus, power supply and some additional VME boards (for instance DRAM 2M and FD/WD) are needed to test full VME bus signal/data transfers. The transfer of data, address signals, interrupt and arbitration logic, I/O transfers, and other functions of the CPU 68Ø1Ø board(s) should be tested.

Several tests of the internal and external functions of the CPU 68Ø1Ø board(s) can be performed in the same way, as explained in the CHAPTER 2. Test of the external DRAM should be performed, to check the data/address signal transfers, parity logic, generation of the SYSCLK signal, etc.

EPROM resident firmware should be replaced with the tests of the (for instance) FD/WD module, or these test can be downloaded with the existing EPROM resident firmware, to fully test the interrupt, arbitration logic and I/O transfers of the CPU 68Ø1Ø board(s).

The CPU 68Ø1Ø board, being tested, should be tested only in the previonsly fully tested system environment.

CHAPTER 5

5. FINAL TEST

For the final go/no go test of the CPU 68Ø1Ø board(s), the previously fully tested CPU board in the stand alone and system environments, should be put in the UNIX or CPM 68/K environments and tested in that environment for some time.

In the UNIX environment the "fsck" system call could be run several times, for instance.

In the CP/M 68K invironment, "pip" of a long file from Winchester to floppy disk and back could be executed for several times, for instance.

After some sort of testing in the real-time environment it can be assured, that the CPU 68Ø1Ø board is functioning properly.

CPU 68Ø1Ø board(s) can now be used to build up new system(s) on the basis on the CPU 68Ø1Ø board.